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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,807	03/10/2004	Dalson Ye Seng Kim	02-1467.1	4520

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STEPHEN A GRATTON
THE LAW OFFICE OF STEVE GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228

EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,807	SENG KIM ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *304,804,205,305*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the preliminary amendment filed 10 March 2004.

Information Disclosure Statement

The information disclosure statement filed 10 March 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 37-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Moden (U.S. Patent 6,310,390).

In regards to claims 17-39, Moden discloses a ball grid array package (Fig. 1c) that contains a metal leadframe (14) having a first side and a second side; attaching a semiconductor die (12) to the first side in a chip on board configuration; bonding a

plurality of interconnects (30) to the die and to the leadframe; and forming a plurality of terminal contacts (28) on leadframe on the second side, an encapsulant (18) on the die, on the interconnects and on the leadframe, the interconnect comprise wires (30) and the wire bonding and the bonding step comprises wire bonding

In regards to claims 40-44, Moden discloses a ball grid array package (Figs. 1c and 3) that contains a chip on board leadframe comprising a plurality of leadfingers (32), a plurality of interconnect bonding sites (26) on a first side thereof and a plurality of terminal bonding sites (28) on a second side thereof in an area array; attaching a back of a semiconductor die (12) to the leadfingers on the first side; bonding a plurality of interconnects (30) to the die and to the interconnect bonding sites; forming a plurality of terminal contacts (16) on the terminal bonding sites; and forming an encapsulant (18) on the die, interconnects and the leadframe, wherein the attaching step comprises forming an adhesive member (36) between the die and the leadframe, wherein forming the terminal contacts step comprises forming or attaching bumps or balls (16) to the terminal bonding sites, the interconnects comprise wires (30) and the bonding step comprises wire bonding and the leadframe is contained on a strip containing a plurality of leadframes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 45-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden in view of Corisis et al (U.S. Publication 2002/0027280).

In regards to claims 45-50 and 57-63, Moden discloses a ball grid array package (Figs. 1c and 3) that contains a chip on board leadframe comprising a plurality of leadfingers (32), a plurality of interconnect bonding sites (26) on a first side thereof and a plurality of terminal bonding sites (28) on a second side thereof in an area array; attaching a back of a semiconductor die (12) to the leadfingers on the first side where the die has circuit side and die contacts; bonding a plurality of interconnects (30) to the die and to the interconnect bonding sites; forming a plurality of terminal contacts (16) on the terminal bonding sites; and forming a molding polymer encapsulant (18) on the die, interconnect and the leadframe, wherein the attaching step comprises forming an adhesive member (36) between the die and the leadframe, wherein forming the terminal contacts step comprises forming or attaching bumps or balls (16) to the terminal bonding sites, the interconnects comprise wires (30), the terminal contacts comprise metal balls (16) and are arranged in a grid array and the encapsulate and leadframe have a chip scale outline. Moden discloses all the limitations except for a bus bar electrically connecting selected leadframes. Whereas Corisis discloses an integrated circuit (Fig. 3) that contains a leadframe with leadfingers (18) with a bus bar (42 (long contact that connects the leadfingers together)), a plurality of interconnects (22), interconnect bonding sites (20), the bus bar can connect along a length, a side or a first side of the leadfingers (Page 3, Paragraph 24) therefore can connect the last two

leadfingers and the interconnects will not cross the bus bar, the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bar is located proximate to an inner portion of the leadframe. The bus bar is formed to electrically connect the leadfingers together to decrease number of buses, which will increase speed and performance and reduce size. (Page 3, Paragraph 24) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Moden by incorporating a bus bar to electrically connect the leadfingers together to decrease number of buses which will increase speed and performance and reduce size as taught by Corisis.

In regards to claims 51-56, Moden discloses a ball grid array package (Figs. 1c and 3) that contains a chip on board leadframe comprising a plurality of leadfingers (32), a plurality of interconnect bonding sites (26) on a first side thereof and a plurality of terminal bonding sites (28) on a second side thereof in an area array; attaching a back of a semiconductor die (12) to the leadfingers on the first side where the die has circuit side and die contacts; bonding a plurality of interconnects (30) to the die and to the interconnect bonding sites; forming a plurality of terminal contacts (16) on the terminal bonding sites; and forming a molding polymer encapsulant (18) on the die and the leadframe, wherein the attaching step comprises forming an adhesive member (36) between the die and the leadframe, wherein forming the terminal contacts step comprises forming or attaching bumps or balls (16) to the terminal bonding sites, the interconnects comprise wires (30), the terminal contacts comprise metal balls (16) and are arranged in a grid array and the leadframe is contained on a strip containing a

plurality of leadframes. Moden discloses all the limitations except for a bus bar electrically connecting selected leadframes. Whereas Corisis discloses an integrated circuit (Fig. 3) that contains a leadframe with a first side, second side, inner portion and outer periphery with leadfingers (18) with a bus bar (42 (long contact that connects the leadfingers together)) located proximate to the inner portion, a plurality of interconnects (22), interconnect bonding sites (20) proximate to the outer periphery, the bus bar can connect along a length, a side or a first side of the leadfingers (Page 3, Paragraph 24) therefore can connect the last two leadfingers and the interconnects will not cross the bus bar, the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bar is located proximate to an inner portion of the leadframe. The bus bar is formed to electrically connect the leadfingers together to decrease number of buses, which will increase speed and performance and reduce size. (Page 3, Paragraph 24) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Moden by incorporating a bus bar to electrically connect the leadfingers together to decrease number of buses which will increase speed and performance and reduce size as taught by Corisis.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Farnworth et al. (U.S. Patent 6,451,624) discloses a semiconductor package with a leadframe, leadfingers, die, interconnect and terminal contacts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KR
KLR

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800